Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1–7 (previously canceled)

Claim 8 (currently amended). An ingress/egress port for an Ethernet switch comprising:

a plurality of Media Access Control (MAC) interfaces, each MAC interface is ~~capable of receiving/transmitting~~ configured to receive/transmit Fast Ethernet (FE) packets, at least one of the MAC interfaces further being ~~configurable~~ configured to receive/transmit Gigabit Ethernet (GE) packets;

receive and transmit modules which are ~~configurable~~ configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces; and

wherein the ingress/egress port ~~is switchable between a first mode and a second mode, in which the ingress/egress port~~ operates as a single GE port in a first ~~the first~~ mode of operation and as more than one FE port in a second ~~the second~~ mode of operation; and

wherein each MAC interface is associated with a separate buffer configured to store packets as they are received at the respective MAC interface, the receive module being arranged to receive packets from the respective buffers sequentially.

Claim 9 (Previously Presented). The ingress/egress port according to claim 8 wherein only one of the MAC interfaces is configured configurable to receive/transmit both GE and FE packets, the other MAC interfaces only being adapted to receive/transmit FE packets.

Claim 10 (Currently Amended). The ingress/egress port according to claim 9 wherein ~~which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby~~ the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

Claim 11 (Currently Amended). The ingress/egress port according to claim 8 wherein ~~which each MAC interface is associated with a buffer configured to store packets as they are received, the receive module being arranged to receive packets from the buffers sequentially, whereby~~ the receive module receives the FE packets sequentially even if FE packets actually reach different ones of the MAC interfaces simultaneously.

Claim 12 (Previously Presented). The ingress/egress port according to claim 8 wherein the receive module further includes a memory configured to store packet data, and a receiver interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

Claim 13 (Currently Amended). The ingress/egress port according to claim 12, wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces, and wherein the receiver interface is further configured ~~operable~~ to fetch packet data from the set of buffers and store the packet data in the memory.

Claim 14 (Previously Presented). The ingress/egress port according to claim 13, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

Claim 15 (Currently Amended). The ingress/egress port according to claim 13, wherein the receiver interface is further configured ~~operable~~ to store the descriptor associated with the packet data in the memory.

Claim 16 (Previously Presented). The ingress/egress port according to claim 8 wherein the plurality of MAC interfaces consists of 8 MAC interfaces.

Claim 17 (currently amended). An Ethernet switch comprising:

at least one ingress/egress port, each ingress/egress port having

a plurality of Media Access Control (MAC) interfaces, each MAC interface is ~~capable of receiving/transmitting~~ configured to receive/transmit Fast Ethernet (FE) packets, at least one of the MAC interfaces further being ~~configurable~~ configured to receive/transmit Gigabit Ethernet (GE) packets;

receive and transmit modules which are ~~configurable~~ configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces; and

wherein the ingress/egress port ~~is switchable between a first mode and a second mode, in which the ingress/egress port~~ operates as a single GE port in a first ~~the first~~ mode of operation and as more than one FE port in a second ~~the second~~ mode of operation; and

wherein each MAC interface is associated with a separate buffer configured to store packets as they are received at the respective MAC interface, the receive module being arranged to receive packets from the respective buffers sequentially.

Claim 18 (cancelled)

Claim 19 (currently amended). The Ethernet switch according to claim 17, wherein the at least one ingress/egress port comprises eight ingress/egress ports, each ingress/egress port being configured to switch ~~switchable~~ between a first mode and a second mode, in which each ingress/egress port operates as a single GE port in the first mode and as eight FE ports in the second mode and wherein the switch can operate as n GE ports and 8(8-n) FE ports for n a selectable integer in the range 0 and 8.

Claim 20 (previously presented). The Ethernet switch according to claim 17, wherein the receive module further includes a memory configured to store packet data, and a receiver

interface configured to extract header data from the packet data and generate a descriptor therefrom, the descriptor associated with the packet data within the receive module.

Claim 21 (currently amended). The Ethernet switch according to claim 20, wherein the receive module further comprises a set of buffers configured to receive packets from at least one of the MAC interfaces, and wherein the receiver interface is further configured ~~operable~~ to fetch packet data from the set of buffers and store the packet data in the memory.

Claim 22 (previously presented). The Ethernet switch according to claim 21, wherein each buffer of the set of buffers comprises a first-in-first-out buffer.

Claim 23 (currently amended). The Ethernet switch according to claim 21, wherein the receiver interface is further configured ~~operable~~ to store the descriptor associated with the packet data in the memory.

Claim 24 (currently amended). A method, comprising

providing data packets to an ingress/egress port of an Ethernet switch, ingress/egress port having a plurality of Media Access Control (MAC) interfaces, each MAC interface configured for ~~capable of~~ receiving/transmitting Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configured ~~configurable~~ to receive/transmit Gigabit Ethernet (GE) packets;

storing the data packets in buffers associated with the plurality of MAC interfaces, each MAC interface being associated with a separate buffer;

passing packet data from the data packets from the buffers to a receive module, the receive module configured ~~configurable~~ to receive both GE and FE packets from all the MAC interfaces;

passing outgoing packet data from a transmit module to the MAC interfaces, the transmit module configured ~~configurable~~ to transmit both GE and FE packets to all the MAC interfaces; and

switching the ingress/egress port between a first mode and a second mode, in which the ingress/egress port operates as a single GE port in the first mode and as more than one FE port in the second mode.

Claim 25 (previously presented). The method according to claim 24, further comprising providing a control signal to determine whether the MAC interfaces operate as FE interfaces or whether the at least one interface operates as a GE interface.

Claim 26 (previously presented). The method according to claim 25, wherein only one of the MAC interfaces is configured ~~configurable~~ to receive/transmit both GE and FE packets, and the other MAC interfaces are only adapted to receive/transmit FE packets.

Claim 27 (previously presented). The method according to claim 24, wherein only one of the MAC interfaces is configured ~~configurable~~ to receive/transmit both GE and FE packets, and the other MAC interfaces are only adapted to receive/transmit FE packets.

Claim 28 (New) An ingress/egress port for an Ethernet switch, the ingress/egress port comprising:

a plurality of Media Access Control (MAC) interfaces, each MAC interface being configured to receive/transmit Fast Ethernet (FE) packets, at least one of the MAC interfaces further being configured to receive/transmit Gigabit Ethernet (GE) packets;

receive and transmit modules which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces; and

a switch configured to switch the ingress/egress port between a first mode and a second mode of operation for the ingress/egress port, wherein the ingress/egress port operates as a single GE port in the first mode of operation using the at least one of the MAC interfaces to transmit and receive GE packets and as more than one FE port in the second mode of operation using the plurality of MAC interfaces to transmit and receive FE packets.

Claim 29 (New) An ingress/egress port for an Ethernet switch, the ingress/egress port comprising:

a plurality of Media Access Control (MAC) interfaces configured to receive/transmit Fast Ethernet (FE) packets;

at least one MAC interface configured to receive/transmit Gigabit Ethernet (GE) packets in a first mode of operation and to receive/transmit FE packets in a second mode of operation; and

receive and transmit modules which are configured respectively to receive both GE and FE packets from, and transmit both GE and FE packets to, all the MAC interfaces;

wherein the ingress/egress port operates as a single GE port in the first mode of operation using the at least one MAC interface to transmit and receive GE packets and as more a plurality of FE ports in the second mode of operation using the plurality and the at least one MAC interface to transmit and receive FE packets.